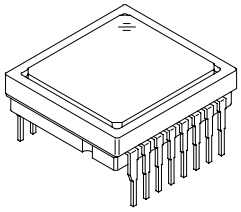
SONY

ICX084AL

1/3-inch Progressive Scan CCD Image Sensor with Square Pixel for B/W Cameras

16 pin DIP (Plastic)



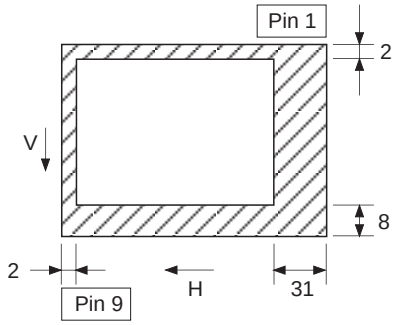
Description

The ICX084AL is a 1/3-inch interline CCD solid-state image sensor with a square pixel array which supports VGA format. Progressive scan allows all pixels signals to be output independently within approximately 1/30 second. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still image without a mechanical shutter. High sensitivity and low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

This chip is suitable for applications such as two-dimensional bar code readers, PC input cameras, etc.

Features

- Progressive scan allows individual readout of the image signals from all pixels.
- High vertical resolution (480 TV-lines) still image without a mechanical shutter.
- Square pixel unit cell
- Supports VGA format
- Horizontal drive frequency: 12.27MHz
- No voltage adjustments (reset gate and substrate bias are not adjusted.)
- High resolution, high sensitivity, low dark current
- Continuous variable-speed shutter
  1/30 (Typ.) to 1/10000s
- Low smear
- Excellent antiblooming characteristics
- Horizontal register: 5V drive
- 16-pin high precision plastic package (enables dual-surface standard)



Optical black position
(Top View)

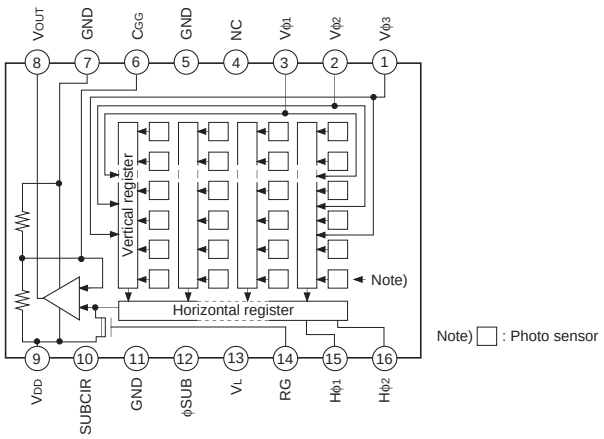
Device Structure

- Interline CCD image sensor
- Optical size: 1/3-inch format
- Number of effective pixels: 659 (H) × 494 (V) approx. 330K pixels
- Total number of pixels: 692 (H) × 504 (V) approx. 350K pixels
- Chip size: 5.84mm (H) × 4.94mm (V)
- Unit cell size: 7.4µm (H) × 7.4µm (V)
- Optical black: Horizontal (H) direction Front 2 pixels, rear 31 pixels
  Vertical (V) direction Front 8 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 16
  Vertical 5
- Substrate material: Silicon

E95307D8X-PS

Block Diagram and Pin Configuration

(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ3	Vertical register transfer clock	9	VDD	Supply voltage
2	Vφ2	Vertical register transfer clock	10	SUBCIR	Supply voltage for the substrate voltage generation
3	Vφ1	Vertical register transfer clock	11	GND	GND
4	NC		12	φSUB	Substrate clock
5	GND	GND	13	VL	Protective transistor bias
6	CGG	Output amplifier gate*1	14	RG	Reset gate clock
7	GND	GND	15	Hφ1	Horizontal register transfer clock
8	VOUT	Signal output	16	Hφ2	Horizontal register transfer clock

*1 DC bias is applied within the CCD, so that this pin should be grounded externally through a capacitance of 1000pF or more.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate clock φSUB – GND		–0.3 to +36	V	
Supply voltage	VDD, VOUT, CGG, SUBCIR – GND	–0.3 to +18	V	
	VDD, VOUT, CGG, SUBCIR – φSUB	–22 to +9	V	
Clock input voltage	Vφ1, Vφ2, Vφ3 – GND	–15 to +16	V	
	Vφ1, Vφ2, Vφ3 – φSUB	to +10	V	
Voltage difference between vertical clock input pins		to +15	V	*2
Voltage difference between horizontal clock input pins		to +16	V	
Hφ1, Hφ2 – Vφ3		–16 to +16	V	
Hφ1, Hφ2 – GND		–10 to +15	V	
Hφ1, Hφ2 – φSUB		–55 to +10	V	
VL – φSUB		–65 to +0.3	V	
Vφ2, Vφ3 – VL		–0.3 to +27.5	V	
RG – GND		–0.3 to +20.5	V	
Vφ1, Hφ1, Hφ2, GND – VL		–0.3 to +17.5	V	
Storage temperature		–30 to +80	°C	
Operating temperature		–10 to +60	°C	

*2 +24V (Max.) when clock width < 10µs, clock duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L	*1				
Substrate clock	φSUB	*2				

*1 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform, or the same power supply as the V_L power supply for the V driver should be used.

*2 Set SUBCIR pin to open when applying a DC bias to the substrate clock pin.

DC Characteristics

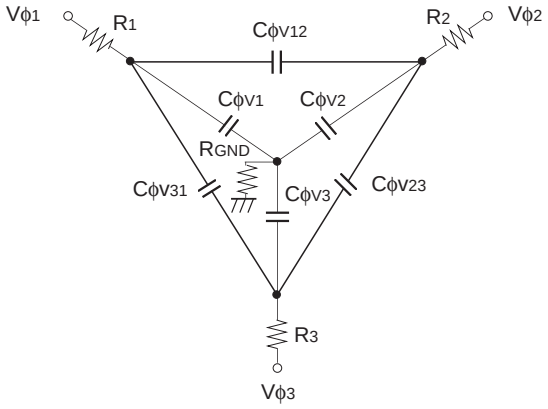
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}		6	8	mA	

Clock Voltage Conditions

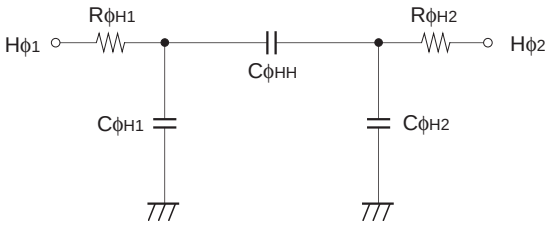
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH02}	–0.05	0	0.05	V	2	$V_{VH} = V_{VH02}$
	V_{VH1}, V_{VH2}, V_{VH3}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}	–8.0	–7.5	–7.0	V	2	$V_{VL} = (V_{VL1} + V_{VL3})/2$
	Vφ1, Vφ2, Vφ3	6.8	7.5	8.05	V	2	
	I V_{VL1}–V_{VL3} I			0.1	V	2	
	V_{VHH}			1.0	V	2	High-level coupling
	V_{VHL}			2.3	V	2	High-level coupling
	V_{VLH}			1.0	V	2	Low-level coupling
	V_{VLL}			1.0	V	2	Low-level coupling
Horizontal transfer clock voltage	Vφ$_H$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
Reset gate clock voltage	Vφ$_{RG}$	4.5	5.0	5.5	V	4	Input through 0.01µF capacitance
	V_{RGLH} – V_{RGLL}			0.8	V	4	Low-level coupling
	V_{RGH}	V_{DD} +0.4	V_{DD} +0.6	V_{DD} +0.8	V	4	
Substrate clock voltage	Vφ$_{SUB}$	21.5	22.5	23.5	V	5	

Clock Equivalent Circuit Constant

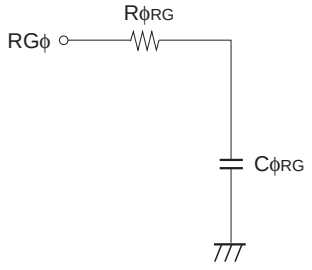
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi V1$		560		pF	
	$C\phi V2$		470		pF	
	$C\phi V3$		1500		pF	
Capacitance between vertical transfer clocks	$C\phi V12$		1500		pF	
	$C\phi V23$		1500		pF	
	$C\phi V31$		1000		pF	
Capacitance between horizontal transfer clock and GND	$C\phi H1$, $C\phi H2$		43		pF	
Capacitance between horizontal transfer clocks	$C\phi HH$		39		pF	
Capacitance between reset gate clock and GND	$C\phi RG$		5		pF	
Capacitance between substrate clock and GND	$C\phi SUB$		570		pF	
Vertical transfer clock series resistor	$R1$, $R2$		20		Ω	
	$R3$		56		Ω	
Vertical transfer clock ground resistor	$RGND$		43		Ω	
Horizontal transfer clock series resistor	$R\phi H1$, $R\phi H2$		10		Ω	
Reset gate clock series resistor	$R\phi RG$		39		Ω	



Vertical transfer clock equivalent circuit



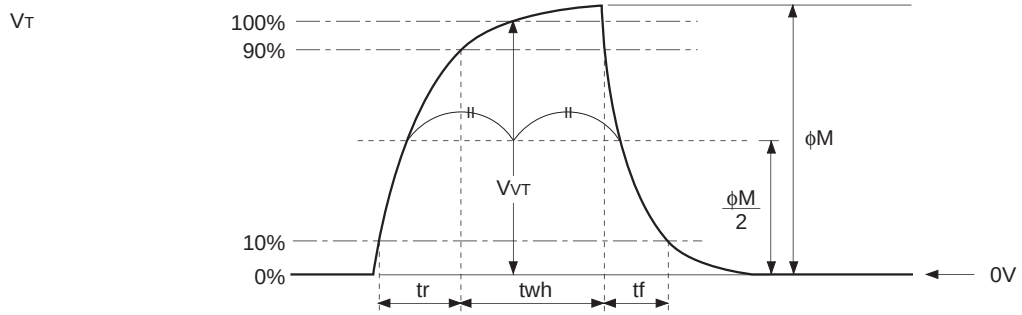
Horizontal transfer clock equivalent circuit



Reset gate clock equivalent circuit

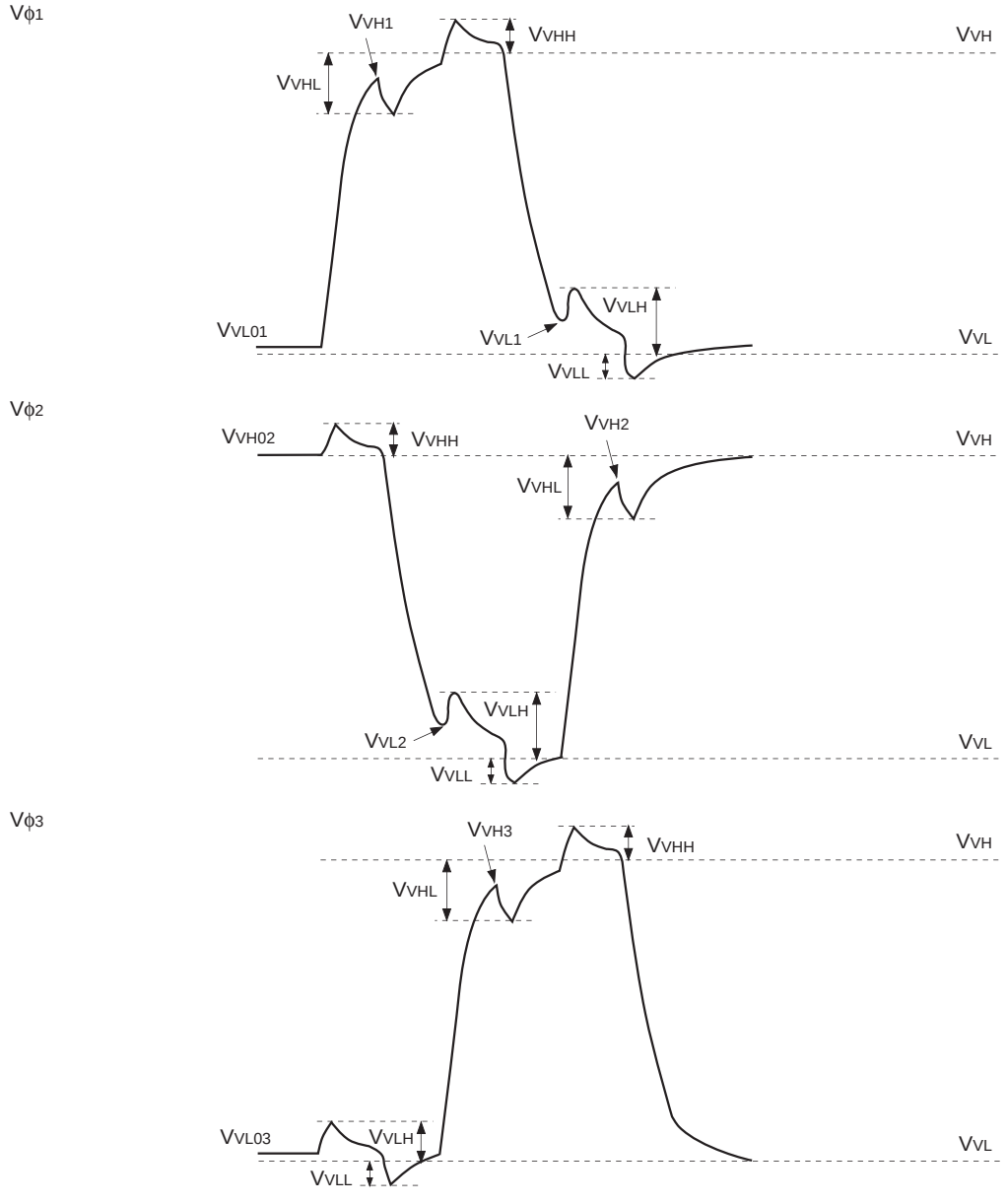
Drive Clock Waveform Conditions

(1) Readout clock waveform



Note) Readout clock is used by composing vertical transfer clocks Vϕ2 and Vϕ3.

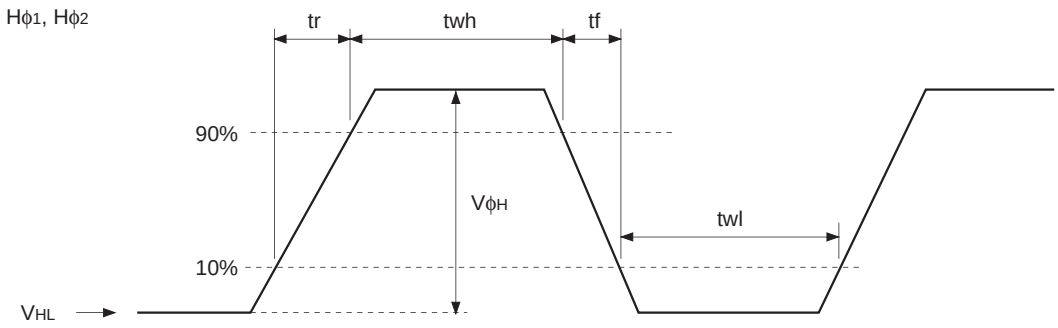
(2) Vertical transfer clock waveform



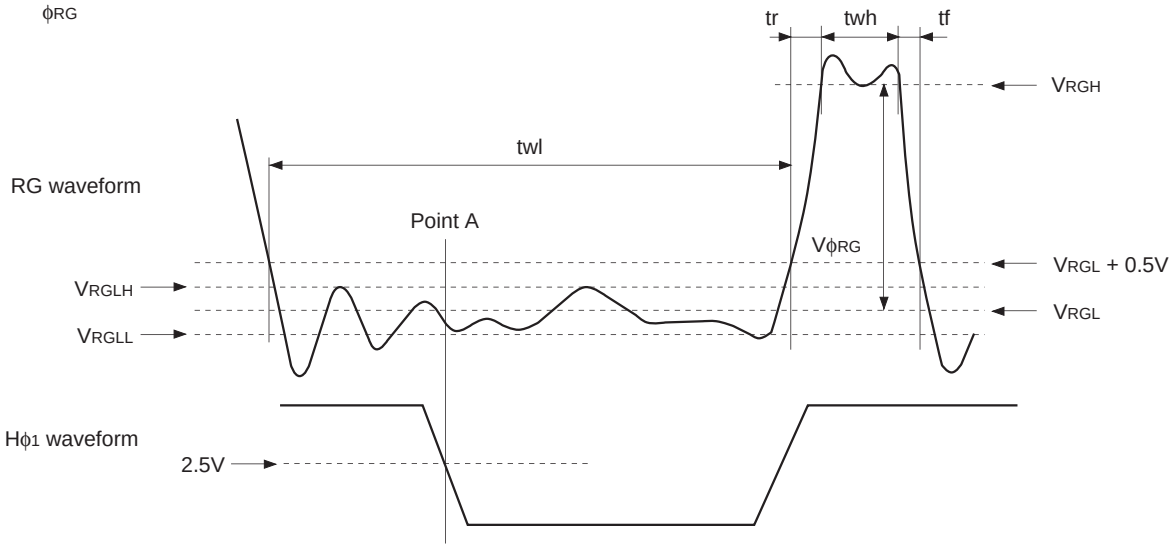
$V_{VH} = V_{VH02}$
$V_{VL} = (V_{VL01} + V_{VL03})/2$
$V_{VL3} = V_{VL03}$

$V_{\phi V1} = V_{VH1} - V_{VL01}$
$V_{\phi V2} = V_{VH02} - V_{VL2}$
$V_{\phi V3} = V_{VH3} - V_{VL03}$

(3) Horizontal transfer clock waveform



(4) Reset gate clock waveform



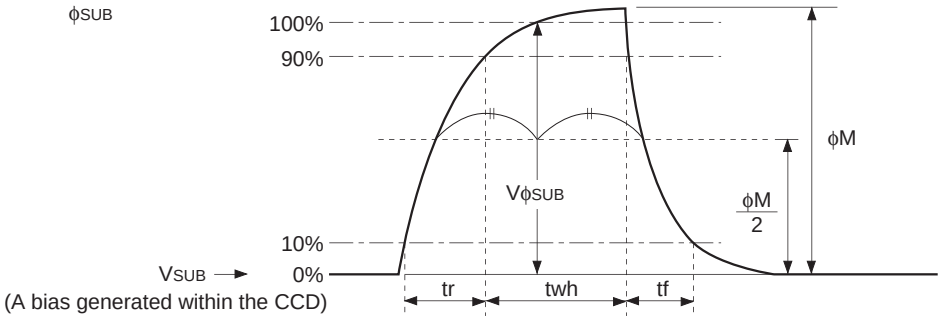
V_{RGLH} is the maximum value and V_{RGLL} is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG. In addition, V_{RGL} is the average value of V_{RGLH} and V_{RGLL}.

$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming V_{RGH} is the minimum value during the interval t_{wh}, then:

$$V_{\phi RG} = V_{RGH} - V_{RGL}$$

(5) Substrate clock waveform



Clock Switching Characteristics

Item		Symbol	twh			twl			tr			tf			Unit	Remarks
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock		V_T	2.3	2.5						0.5			0.5		µs	During readout
Vertical transfer clock		$V\phi_1$, $V\phi_2$, $V\phi_3$										15		350	ns	*1
Horizontal transfer clock	During imaging	$H\phi_1$	24	30		25	31.5			10	17.5		10	17.5	ns	*2
		$H\phi_2$	26.5	31.5		25	30			10	15		10	15		
	During parallel-serial conversion	$H\phi_1$								0.01			0.01		µs	
		$H\phi_2$								0.01			0.01			
Reset gate clock		ϕ_{RG}	11	13			62.5			3			3		ns	
Substrate clock		ϕ_{SUB}	1.5	1.8							0.5			0.5	µs	During drain charge

*1 When vertical transfer clock driver CXD1267AN is used.

*2 tf ≥ tr – 2ns, and the cross-point voltage (V_{CR}) for the $H\phi_1$ rising side of the $H\phi_1$ and $H\phi_2$ waveforms must be at least 2.5V.

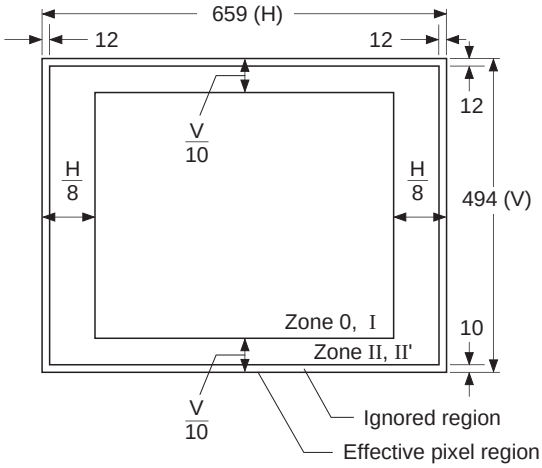
Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1$, $H\phi_2$	21.5	25.5		ns	*3

*3 The overlap period for twh and twl of horizontal transfer clocks $H\phi_1$ and $H\phi_2$ is two.

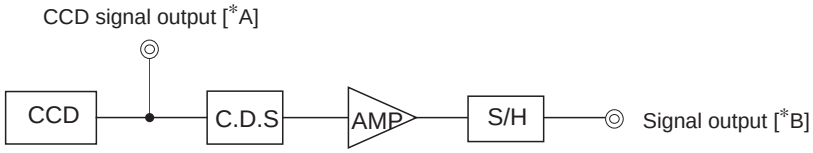
Image Sensor Characteristics (Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	540	700		mV	1	
Saturation signal	Vsat	500			mV	2	Ta = 60°C
Smear	Sm		0.005	0.015	%	3	
Video signal shading	SH			20	%	4	Zone 0 and I
				25	%	4	Zone 0 to II'
Dark signal	Vdt			4	mV	5	Ta = 60°C
Dark signal shading	ΔVdt			1	mV	6	Ta = 60°C
Lag	Lag			0.5	%	7	

Zone Definition of Video Signal shading



Measurement System



Note) Adjust the amplifier gain so that the gain between [*A] and [*B] equals 1.

Image Sensor Characteristics Measurement Method

◎ **Measurement conditions**

1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions.

2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value measured at point [*B] of the measurement system.

◎ **Definition of standard imaging conditions**

1) Standard imaging condition I:
Use a pattern box (luminance : 706cd/m^2, color temperature of 3200K halogen source) as a subject. (pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/250s, measure the signal output (V_S) at the center of the screen, and substitute the value into the following formula.

$$S = V_S \times \frac{250}{30} \text{ [mV]}$$

2. Saturation signal
Set to standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with the average value of the signal output, 150mV, measure the minimum value of the signal output.

3. Smear
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the luminous intensity to 500 times the intensity with the average value of the signal output, 150mV. Then after the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (Vsm [mV]) of the signal output and substitute the value into the following formula.

$$Sm = \frac{Vsm}{150} \times \frac{1}{500} \times \frac{1}{10} \times 100 \text{ [\%] (1/10V method conversion value)}$$

4. Video signal shading
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 150mV. Then measure the maximum (Vmax [mV]) and minimum (Vmin [mV]) values of the signal output and substitute the values into the following formula.

$$SH = (Vmax - Vmin)/150 \times 100 \text{ [\%]}$$

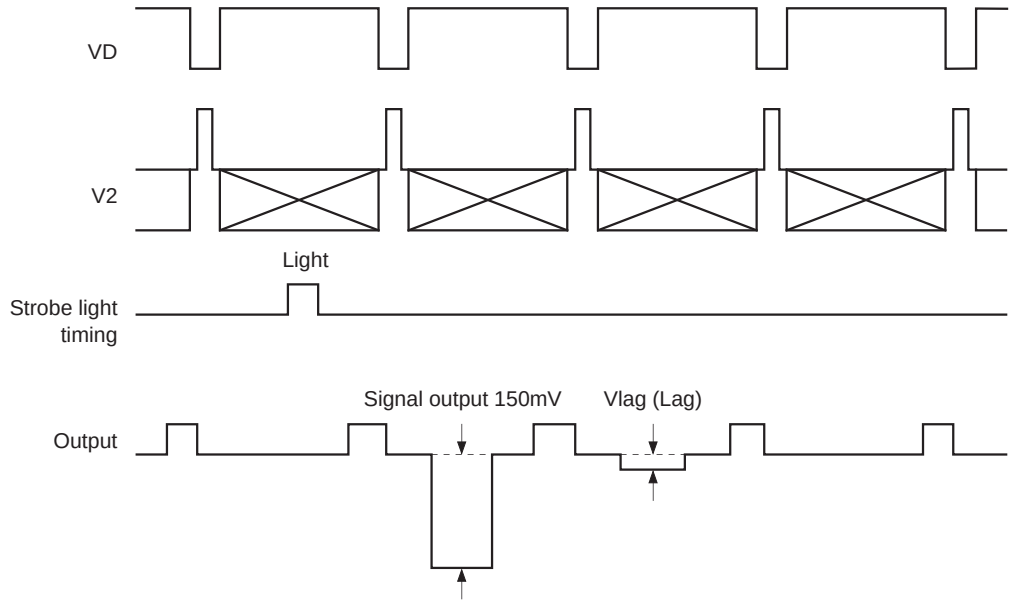
5. Dark signal
Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

6. Dark signal shading
   After measuring 5, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

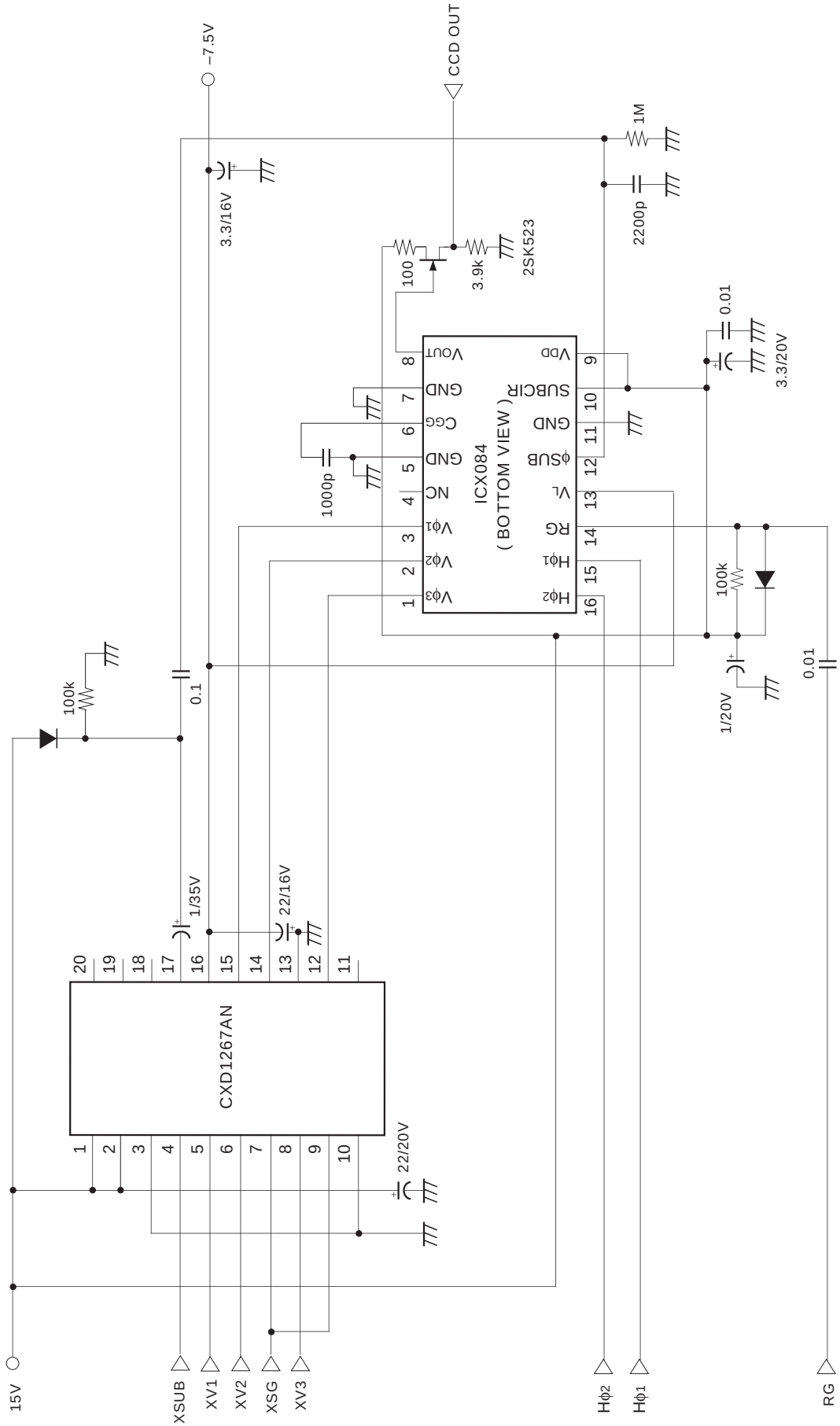
   $\Delta Vdt = Vdmax - Vdmin$ [mV]

7. Lag
   Adjust the signal output value generated by strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

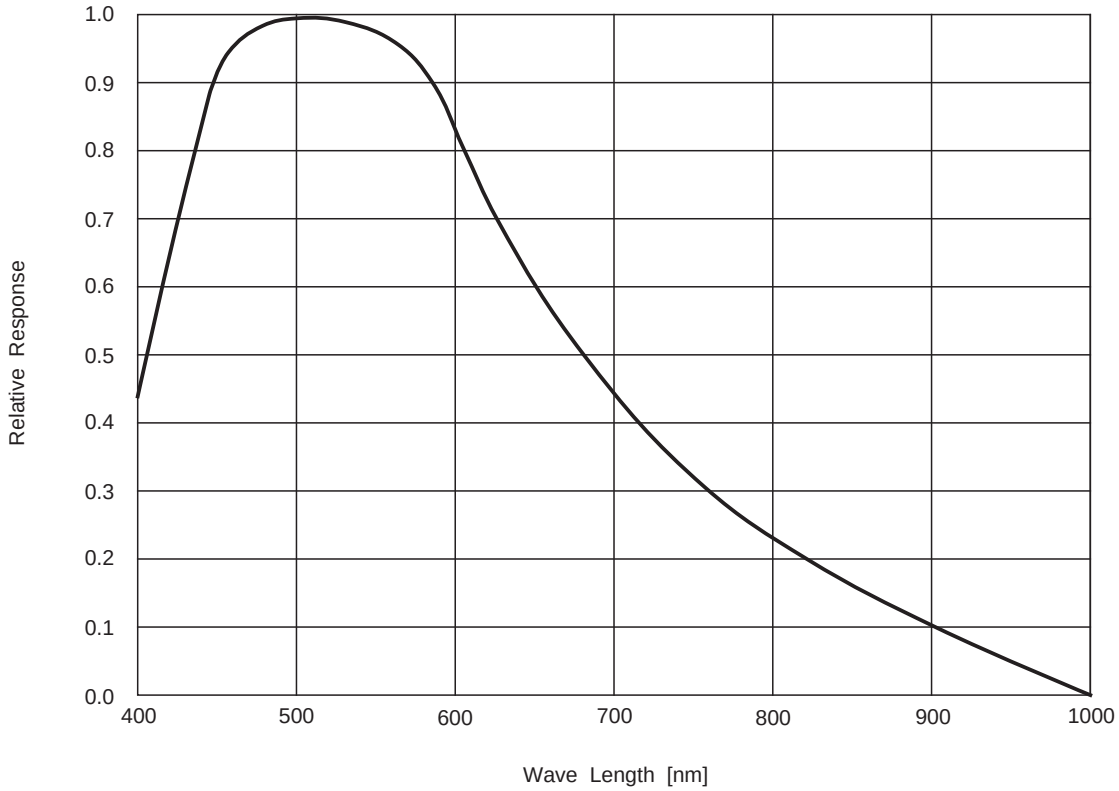
   $Lag = (Vlag/150) \times 100$ [%]



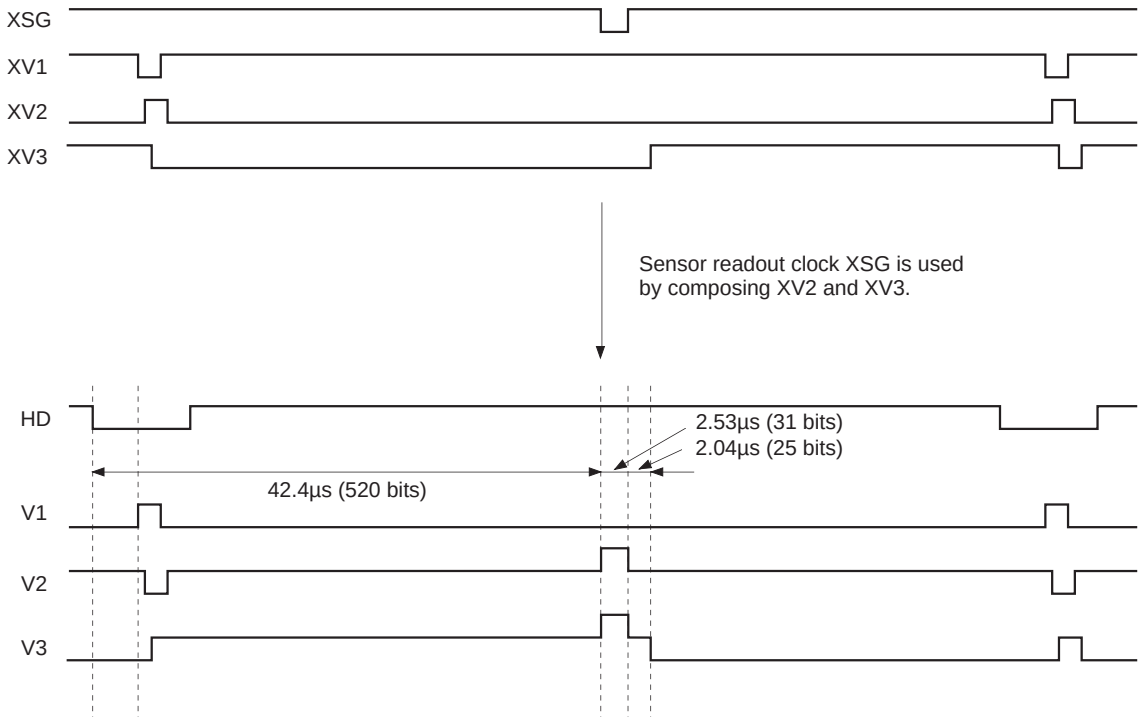
Drive Circuit



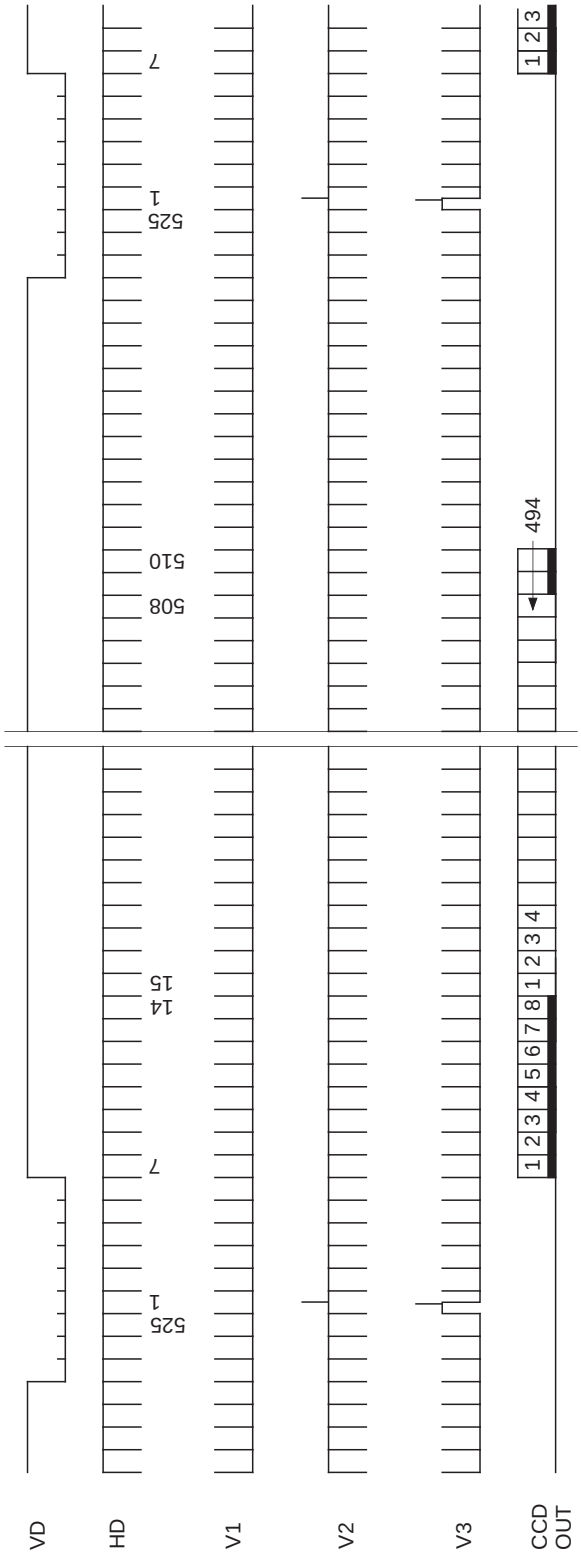
Spectral Sensitivity Characteristics (Includes lens characteristics, excludes light source characteristics)



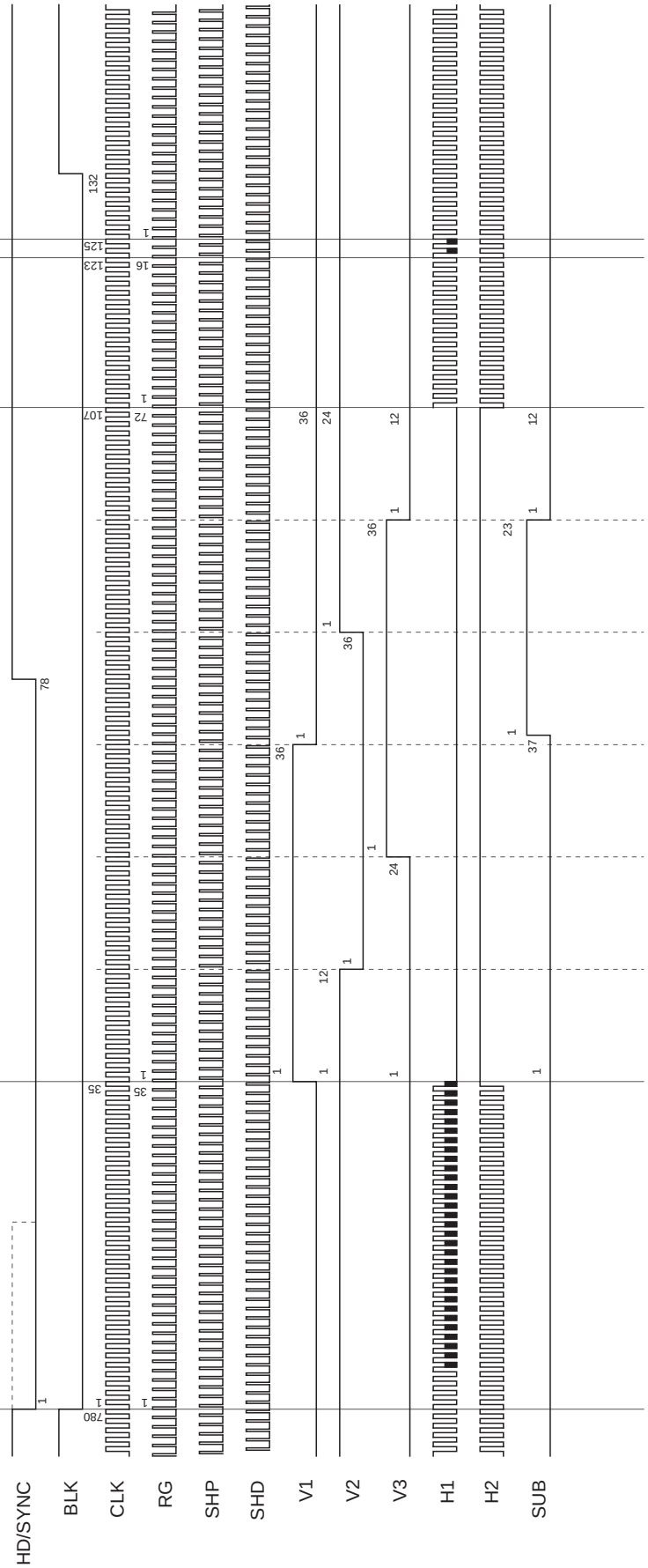
Sensor Readout Clock Timing Chart



Drive Timing Chart (Vertical Sync)



Drive Timing Chart (Horizontal Sync)



Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non-chargeable gloves, clothes or material.
Also use conductive shoes.

b) When handling directly use an earth band.

c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d) Ionized air is recommended for discharge when handling CCD image sensor.

e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering

a) Make sure the package temperature does not exceed 80°C.

b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.

c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection

Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.

a) Perform all assembly operations in a clean room (class 1000 or less).

b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)

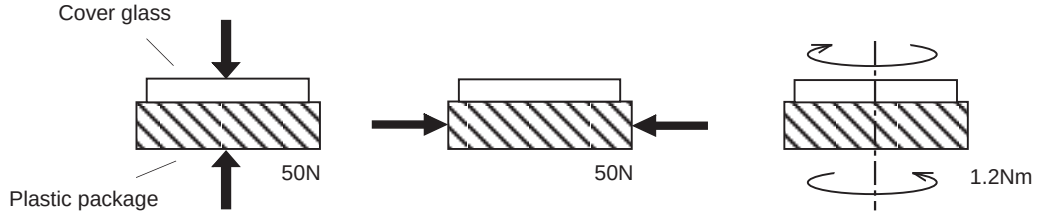
c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.

d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)

a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



Compressive strength **Torsional strength**

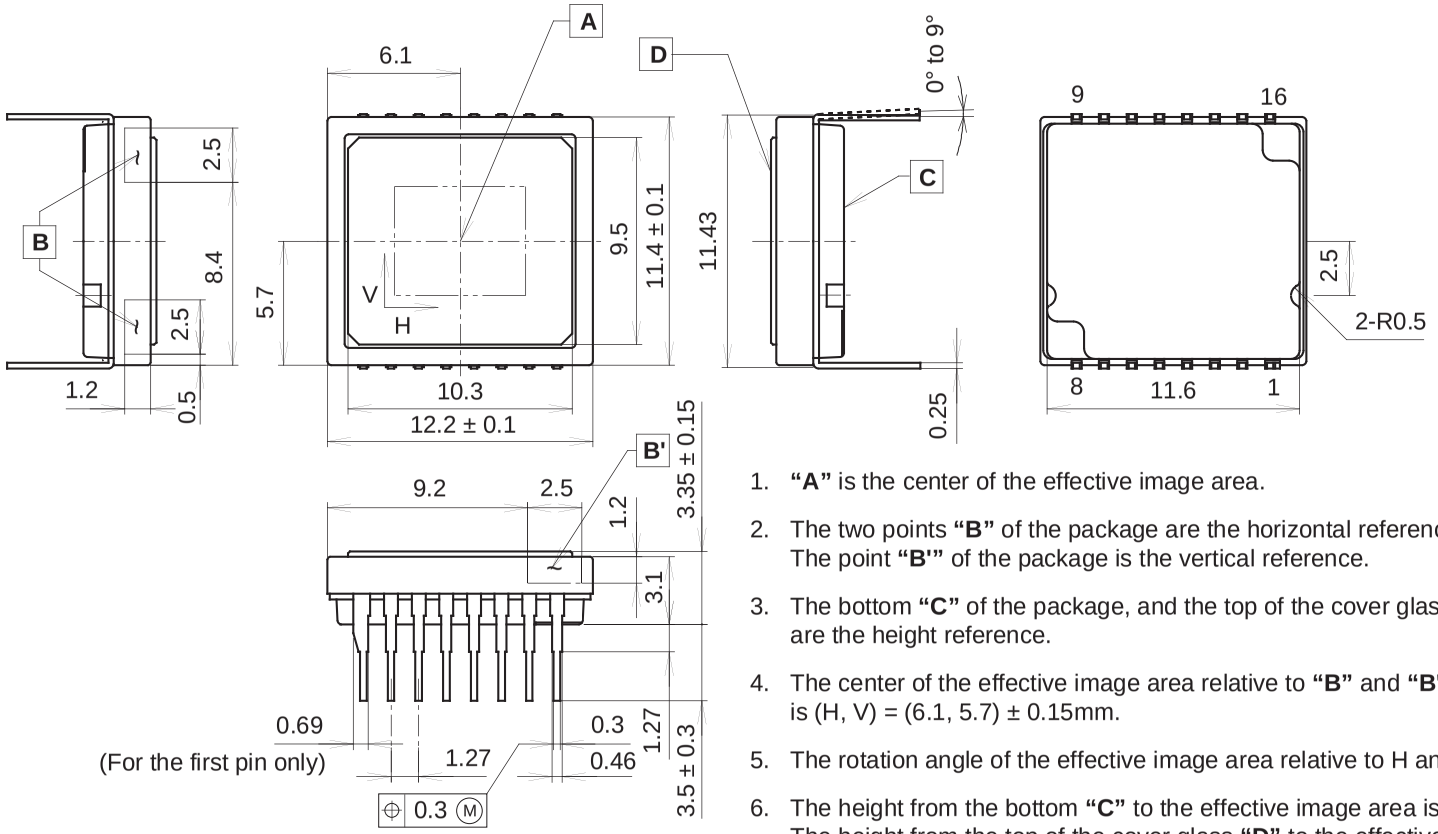
b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.

c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to the other locations as a precaution.
d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.
e) If the lead bend repeatedly and the metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.
f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyano-acrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5) Others
a) Do not expose to strong light (sun rays) for long periods. For continuous using under cruel condition exceeding the normal using condition, consult our company.
b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
c) The brown stain may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.

Package Outline Unit: mm

16pin DIP (450mil)



1. **"A"** is the center of the effective image area.
2. The two points **"B"** of the package are the horizontal reference.
   The point **"B'"** of the package is the vertical reference.
3. The bottom **"C"** of the package, and the top of the cover glass **"D"** are the height reference.
4. The center of the effective image area relative to **"B"** and **"B'"** is (H, V) = (6.1, 5.7) ± 0.15mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom **"C"** to the effective image area is 1.41 ± 0.10mm.
   The height from the top of the cover glass **"D"** to the effective image area is 1.94 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom **"C"** is less than 50µm.
   The tilt of the effective image area relative to the top **"D"** of the cover glass is less than 50µm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.
9. The notches on the bottom of the package are used only for directional index, they must not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.9g